

Amendments to the Claims

This listing of claims will replace all prior versions, and listings of claims in the application:

Listing of Claims:

Claim 1 (Currently Amended): A voltage level shifting circuit comprising:

a first power supply node supplied with a first power supply potential level;

a second power supply node supplied with a second power supply potential level higher than the first power supply potential level;

a third power supply node supplied with a third power supply potential level higher than the second power supply potential level;

a signal input circuit which is coupled between the first power supply node and the second power supply node, which receives a signal having the first and second power supply potential levels, and which outputs complementary signals having the first and second power supply potential levels;

a complimentary signal input circuit which is coupled to the first power supply node and which includes a pair of first MOS transistors, each of the first MOS transistors has a first withstand voltage and has a first electrode coupled to the first power supply node, a second electrode, and a gate electrode receiving one of the complementary signals;

a load circuit which is coupled to the third power supply node and which includes a pair of second MOS transistors, each of the second MOS transistors has a second withstand voltage higher than the first withstand voltage and has a first electrode coupled to the third power supply node, a second electrode, and a gate electrode;

a first voltage down-converting circuit which is coupled between the load circuit and the complimentary signal input circuit, and which prevents a potential level exceeding the first withstand voltage from being supplied to the complimentary signal input circuit;

a third MOS transistor which is coupled between the third power supply node and an output node, which has the second withstand voltage, and which electrically connects the third power supply node to the output node in response to a voltage potential output from the load circuit;

a fourth MOS transistor which is coupled between the first power supply node and the output node, which has the first withstand voltage, which has a gate directly coupled to one of the complimentary signals, and which electrically connects the first power supply node to the output node in response to ~~one of the~~ a voltage potential ~~potentials~~ of the one of the complimentary signals; and

a second voltage down-converting circuit which is coupled between the third MOS transistor and the fourth MOS transistor and which prevents a potential level exceeding the first withstand voltage from being supplied to the fourth MOS transistor.

Claim 2 (Previously Presented): The voltage level shifting circuit according to Claim 1, wherein the first voltage down-converting circuit comprises a pair of fifth MOS transistors, each of which has a first electrode coupled to the load circuit, a second electrode coupled to the corresponding second electrodes of the first MOS transistors, and a gate electrode supplied with a fixed voltage potential level.

Claim 3 (Original): The voltage level shifting circuit according to Claim 2, wherein the fixed voltage potential level is the second power supply potential level.

Claim 4 (Original): The voltage level shifting circuit according to Claim 1, wherein the second voltage down-converting circuit comprises a sixth MOS transistor which has a first electrode coupled to the third MOS transistor, a second electrode coupled to the fourth MOS transistor, and a gate electrode supplied with a fixed voltage potential level.

Claim 5 (Original): The voltage level shifting circuit according to Claim 4, wherein the fixed voltage potential level is the second power supply potential level.

Claim 6 (Currently Amended): A ~~[[The]]~~ voltage level shifting circuit ~~according to Claim 4~~
comprising:

a first power supply node supplied with a first power supply potential

level;

a second power supply node supplied with a second power supply potential level higher than the first power supply potential level;

a third power supply node supplied with a third power supply potential level higher than the second power supply potential level;

a signal input circuit which is coupled between the first power supply node and the second power supply node, which receives a signal having the first and second power supply potential levels, and which outputs complementary signals having the first and second power supply potential levels;

a complimentary signal input circuit which is coupled to the first power supply node and which includes a pair of first MOS transistors, each of the first MOS transistors has a first withstand voltage and has a first electrode coupled to the first power supply node, a second electrode, and a gate electrode receiving one of the complementary signals;

a load circuit which is coupled to the third power supply node and which includes a pair of second MOS transistors, each of the second MOS transistors has a second withstand voltage higher than the first withstand voltage and has a first electrode coupled to the third power supply node, a second electrode, and a gate electrode;

a first voltage down-converting circuit which is coupled between the load circuit and the complimentary signal input circuit, and which prevents a potential

level exceeding the first withstand voltage from being supplied to the complimentary signal input circuit;

a third MOS transistor which is coupled between the third power supply node and an output node, which has the second withstand voltage, and which electrically connects the third power supply node to the output node in response to a voltage potential output from the load circuit;

a fourth MOS transistor which is coupled between the first power supply node and the output node, which has the first withstand voltage, and which electrically connects the first power supply node to the output node in response to one of voltage potentials of the complimentary signals; and

a second voltage down-converting circuit which is coupled between the third MOS transistor and the fourth MOS transistor and which prevents a potential level exceeding the first withstand voltage from being supplied to the fourth MOS transistor,
wherein the pair of second MOS transistors constitute a current mirror load.

Claim 7 (Currently Amended): A ~~[[The]]~~ voltage level shifting circuit ~~according to Claim 1, further comprising~~ comprising:

a first power supply node supplied with a first power supply potential level;

a second power supply node supplied with a second power supply potential level higher than the first power supply potential level;

a third power supply node supplied with a third power supply potential level higher than the second power supply potential level;

a signal input circuit which is coupled between the first power supply node and the second power supply node, which receives a signal having the first and second power supply potential levels, and which outputs complementary signals having the first and second power supply potential levels;

a complimentary signal input circuit which is coupled to the first power supply node and which includes a pair of first MOS transistors, each of the first MOS transistors has a first withstand voltage and has a first electrode coupled to the first power supply node, a second electrode, and a gate electrode receiving one of the complementary signals;

a load circuit which is coupled to the third power supply node and which includes a pair of second MOS transistors, each of the second MOS transistors has a second withstand voltage higher than the first withstand voltage and has a first electrode coupled to the third power supply node, a second electrode, and a gate electrode;

a first voltage down-converting circuit which is coupled between the load circuit and the complimentary signal input circuit, and which prevents a potential level exceeding the first withstand voltage from being supplied to the complimentary signal input circuit;

a third MOS transistor which is coupled between the third power supply node

and an output node, which has the second withstand voltage, and which electrically connects the third power supply node to the output node in response to a voltage potential output from the load circuit;

a fourth MOS transistor which is coupled between the first power supply node and the output node, which has the first withstand voltage, and which electrically connects the first power supply node to the output node in response to one of voltage potentials of the complimentary signals;

a second voltage down-converting circuit which is coupled between the third MOS transistor and the fourth MOS transistor and which prevents a potential level exceeding the first withstand voltage from being supplied to the fourth MOS transistor;
and

a constant current element which is coupled between the first electrodes of the first MOS transistors and the first power supply node.

Claim 8 (Original): The voltage level shifting circuit according to Claim 7, wherein the constant current element comprises a MOS transistor.

Claim 9 (Currently Amended): A voltage level shift circuit comprising:

a first power supply node supplied with a first power supply potential level;

a second power supply node supplied with a second power supply potential level higher than the first power supply potential level;

a third power supply node supplied with a third power supply potential level higher than the second power supply potential level;

a signal input circuit which is coupled between the first power supply node and the second power supply node, which receives a signal having the first and second power supply potential levels, and which outputs complementary signals having the first and second power supply potential levels;

a complimentary signal input circuit which is coupled to the first power supply node and which includes a pair of first MOS transistors, each of the first MOS transistors has a first withstand voltage and has a first electrode coupled to the first power supply node, a second electrode, and a gate electrode receiving one of the complementary signals;

a load circuit which is coupled to the third power supply node and which includes a pair of second MOS transistors, each of the second MOS transistors has a second withstand voltage higher than the first withstand voltage and has a first electrode coupled to the third power supply node, a second electrode, and a gate electrode;

a first voltage descending circuit which is coupled between the load circuit and the complimentary signal input circuit, and which prevents a potential level exceeding the first withstand voltage from being supplied to the complimentary signal input circuit;

a third MOS transistor which is coupled between the third power supply node and an output node, which has the second withstand voltage, and which electrically

connects the third power supply node to the output node in response to a voltage potential output from the load circuit;

a fourth MOS transistor which is coupled between the first power supply node and the output node, which has the first withstand voltage, which has a gate directly coupled to one of the complimentary signals, and which electrically connects the first power supply node to the output node in response to ~~one of the voltage potential~~ potentials of the one of the complimentary signals; and

a second voltage descending circuit which is coupled between the third MOS transistor and the fourth MOS transistor and which prevents a potential level exceeding the first withstand voltage from being supplied to the fourth MOS transistor.

Claim 10 (Previously Presented): The voltage level shifting circuit according to Claim 9, wherein the first voltage descending circuit comprises a pair of fifth MOS transistors, each of which has a first electrode coupled to the load circuit, a second electrode coupled to the corresponding second electrodes of the first MOS transistors, and a gate electrode supplied with a fixed voltage potential level.

Claim 11 (Original): The voltage level shift circuit according to Claim 10, wherein the fixed voltage potential level is the second power supply potential level.

Claim 12 (Previously Presented): The voltage level shift circuit according to Claim 9,

wherein the second voltage descending circuit comprises a sixth MOS transistor which has a first electrode coupled to the third MOS transistor, a second electrode coupled to the fourth MOS transistor, and a gate electrode supplied with a fixed voltage potential level.

Claim 13 (Original): The voltage level shift circuit according to Claim 12, wherein the fixed voltage potential level is the second power supply potential level.

Claim 14 (Currently Amended): A [[The]] voltage level shift circuit according to Claim 9 comprising:

a first power supply node supplied with a first power supply potential level;

a second power supply node supplied with a second power supply potential level higher than the first power supply potential level;

a third power supply node supplied with a third power supply potential level higher than the second power supply potential level;

a signal input circuit which is coupled between the first power supply node and the second power supply node, which receives a signal having the first and second power supply potential levels, and which outputs complementary signals having the first and second power supply potential levels;

a complimentary signal input circuit which is coupled to the first power supply node and which includes a pair of first MOS transistors, each of the first MOS

transistors has a first withstand voltage and has a first electrode coupled to the first power supply node, a second electrode, and a gate electrode receiving one of the complementary signals;

a load circuit which is coupled to the third power supply node and which includes a pair of second MOS transistors, each of the second MOS transistors has a second withstand voltage higher than the first withstand voltage and has a first electrode coupled to the third power supply node, a second electrode, and a gate electrode;

a first voltage descending circuit which is coupled between the load circuit and the complimentary signal input circuit, and which prevents a potential level exceeding the first withstand voltage from being supplied to the complimentary signal input circuit;

a third MOS transistor which is coupled between the third power supply node and an output node, which has the second withstand voltage, and which electrically connects the third power supply node to the output node in response to a voltage potential output from the load circuit;

a fourth MOS transistor which is coupled between the first power supply node and the output node, which has the first withstand voltage, and which electrically connects the first power supply node to the output node in response to one of voltage potentials of the complimentary signals; and

a second voltage descending circuit which is coupled between the third MOS transistor and the fourth MOS transistor and which prevents a potential level exceeding

the first withstand voltage from being supplied to the fourth MOS transistor,
wherein the pair of second MOS transistors constitute a current mirror load.

Claim 15 (Currently Amended): A [[The]] voltage level shift circuit according to Claim 9,
~~further comprising~~ comprising:

a first power supply node supplied with a first power supply potential level;

a second power supply node supplied with a second power supply potential level
higher than the first power supply potential level;

a third power supply node supplied with a third power supply potential level
higher than the second power supply potential level;

a signal input circuit which is coupled between the first power supply node and
the second power supply node, which receives a signal having the first and second
power supply potential levels, and which outputs complementary signals having the first
and second power supply potential levels;

a complimentary signal input circuit which is coupled to the first power supply
node and which includes a pair of first MOS transistors, each of the first MOS
transistors has a first withstand voltage and has a first electrode coupled to the first
power supply node, a second electrode, and a gate electrode receiving one of the
complementary signals;

a load circuit which is coupled to the third power supply node and which includes
a pair of second MOS transistors, each of the second MOS transistors has a second

withstand voltage higher than the first withstand voltage and has a first electrode coupled to the third power supply node, a second electrode, and a gate electrode;

a first voltage descending circuit which is coupled between the load circuit and the complimentary signal input circuit, and which prevents a potential level exceeding the first withstand voltage from being supplied to the complimentary signal input circuit;

a third MOS transistor which is coupled between the third power supply node and an output node, which has the second withstand voltage, and which electrically connects the third power supply node to the output node in response to a voltage potential output from the load circuit;

a fourth MOS transistor which is coupled between the first power supply node and the output node, which has the first withstand voltage, and which electrically connects the first power supply node to the output node in response to one of voltage potentials of the complimentary signals;

a second voltage descending circuit which is coupled between the third MOS transistor and the fourth MOS transistor and which prevents a potential level exceeding the first withstand voltage from being supplied to the fourth MOS transistor; and

a constant current element which is coupled between the first electrodes of the first MOS transistors and the first power supply node.

Claim 16 (Original): The voltage level shift circuit according to Claim 15, wherein the

constant current element comprises a MOS transistor.